Amendments to the Specification:

Please replace paragraph [0022] with the following amended paragraph:

[00022] The disclosed invention includes a method and apparatus for hierarchical Z buffering and stenciling that compares an input tile Z value range with a hierarchical Z value range and a stencil code. The method and apparatus also updates the hierarchical Z value range and stencil code in response to the comparison and determines whether to render a plurality of pixels within the input tile based on the comparison of the input tile Z value range with the hierarchical Z value range and stencil code. In determining whether to render the plurality of pixels within the tile, two different tests are performed, a stencil test and a hierarchical Z value test, otherwise known as a depth test. If the stencil test fails or the hierarchical Z value test fails, a determination is made to not render the pixels, otherwise referred to a killing the tile, as it is determined that the pixels are not visible in the graphical output. It should be noted that the stencil values may need to be changed, even when the tile is killed because the depth and pixel color will not change. If the stencil test passes and the hierarchical Z test passes, the pixels within the tile are rendered, as it is determined that there is a likelihood the pixels within the tile will be visible.

Please replace paragraph [0028] with the following amended paragraph:

[00028] FIG. 3 illustrates a functional block diagram of a portion of the video graphics processor 120 in accordance with one embodiment of the present invention. The processor includes a primitive assembly 130 which receives vertices 132 of video information. The primitive assembly 130 produces a plurality of triangles 134 which are provided to a tile walker 136. The tile walker 136 walks the tile thereupon producing barycentric coordinates 138, the tile

having a plurality of pixels with the plurality of pixels having a plurality of x,y coordinate addresses and a z plane 140.